Ordering number : EN4543

No. 4543

SANYO

LC89925, 89925M

PAL 1H Delay Line

Overview

The LC89925 and LC89925M are delay lines and produce a 1H delayed signal for the PAL format, with an external low-pass filter.

Functions

- 566-stage shift register that can be switched to function as a 562-stage shift register
- Auto-bias circuit
- Sync tip clamp circuit
- Sample-and-hold circuit
- Delay time switching circuit

Features

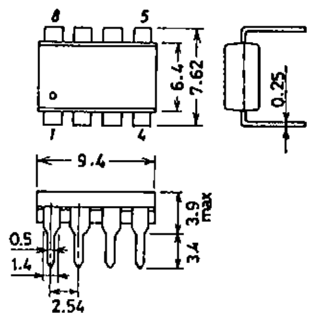
- Single 5 V power supply
- Operates on a low-amplitude clock input.
- Operates with minimal external circuits since peripheral circuits are built in.
- Positive phase signal input, positive phase signal output
- Can be switched (with a control pin input) to produce an NTSC format 1H delayed signal.

Package Dimensions

unit: mm

3001B-DIP8

[LC89925]

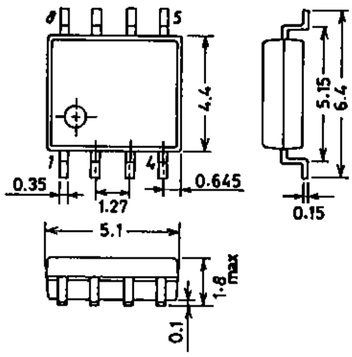


SANYO: DIP8

unit: mm

3032B-MFP8

[LC89925M]



SANYO: MFP8

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.0	V
Allowable power dissipation	Pd max	LC89925	400	mW
		LC89925M	140	mW
Operating temperature	Topr		–10 to +60	°C
Storage temperature	Tstg		–55 to +150	°C

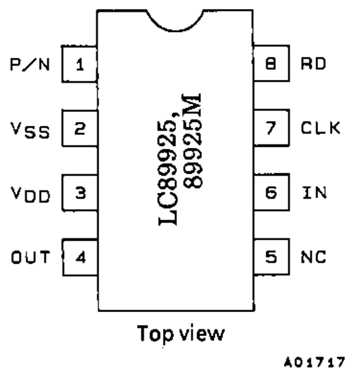
SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Clock input amplitude	V_{CLK}	Sine wave	100	300	1000	mVp-p
Clock frequency	F_{CLK}			8.8672375		MHz
Signal input amplitude	V_{IN}	*		500		mVp-p

Note: * Since sync tip clamping is normally performed, the input signal must be connected in a low impedance state.

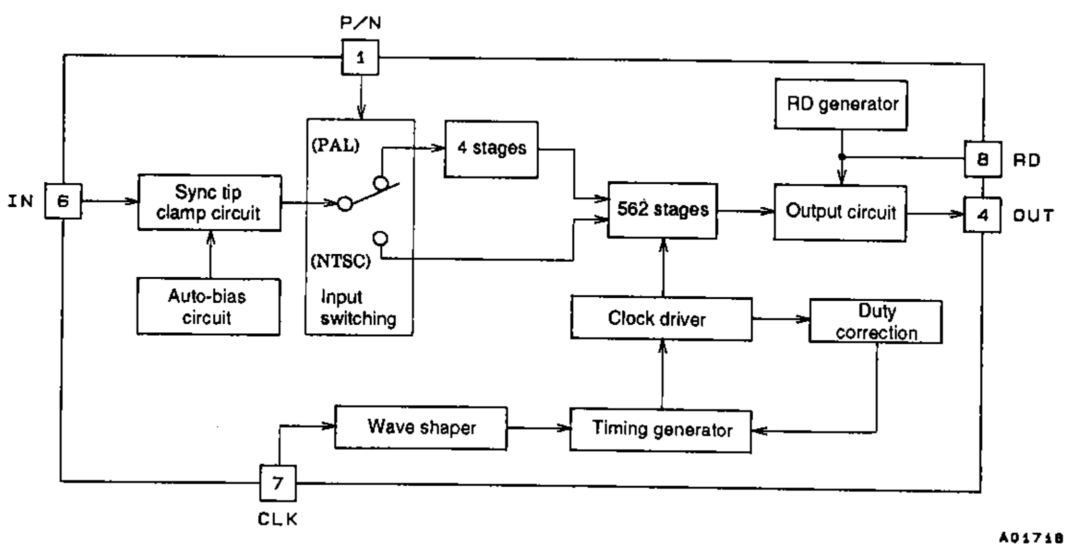
Pin Assignment



Pin Functions

Pin No.	Symbol	Function
1	P/N	Delay time switching
2	V_{SS}	GND
3	V_{DD}	Power supply
4	OUT	Delayed signal output
5	NC	
6	IN	Signal input
7	CLK	Clock input
8	RD	High voltage generator output for Reset Drain

Block Diagram



Functional Description

The delay time is switched by the state of the P/N control pin (pin 1).

0 V: PAL mode

In this mode, the LC89925 provides a PAL 1H (64.0 µs) delay using a 566-stage delay line.

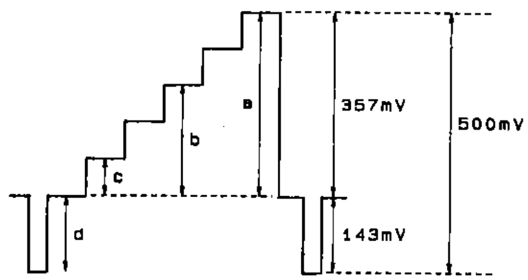
5 V: NTSC mode

In this mode, the LC89925 provides an NTSC 1H (63.5 µs) delay using a 562-stage delay line.

Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0 V, CLK = 8.8672375 MHz; 300 mVp-p; sine wave

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current	I_{DD}	No signal input	5	10	15	mA
Voltage gain	G_V	With a 200 kHz 0.5 Vp-p input	2.5	4.5	6.5	dB
Frequency response	G_f	3.0 MHz, 0.2 Vp-p/200 kHz, 0.2 Vp-p	–3.0	–2.0		dB
Linearity	L6	*	56	60	64	%
	L2	*	18	20	22	%
	L_S	*	37	40	43	%
Clock leakage	L_{CLK}	No signal input, the 2 fsc component		10	30	mVrms
Noise level	N_O	No signal input, 4.2 MHz bandwidth		0.7	2.0	mVrms
Output impedance	Z_O		200	300	400	Ω
Delay time	$T_{D\text{-}P}$			63.91		µs
	$T_{D\text{-}N}$			63.47		µs

Note: * Input signal/output signal



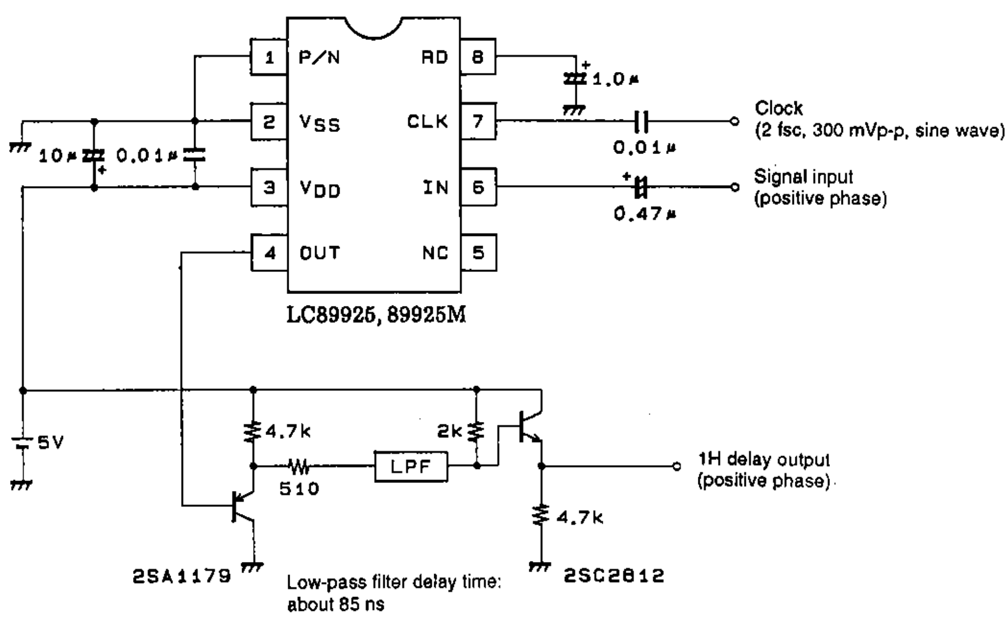
$$L6 = \frac{b}{a}$$

$$L2 = \frac{c}{a}$$

$$L_S = \frac{d}{a}$$

A01719

Sample Application Circuit



A01720

Units (resistance: Ω, capacitance: F)